What is claimed is:

1. An apparatus, comprising:

- an inverting first matching stage responsive to an input clock signal to generate a first inverted signal having a first matching delay, the first matching delay being a difference between a first rise and a first fall propagation time of the first matching stage; and

- an inverting first pull-up stage coupled to the first matching stage and responsive to the first inverted signal to generate a second inverted signal having a first pull-up delay which is substantially reduced by the first matching delay, the first pull-up delay being a difference between a second rise and a second fall propagation time of the first pull-up stage.

2. The apparatus according to claim 1, wherein the first matching stage includes a non-inverting logic element having an input to receive the input clock signal and a NOR gate with one input connected to the input of the non-inverting logic element and another input connected to an output of the non-inverting logic element.

3. The apparatus according to claim 2, wherein the non-inverting logic element includes at least two cascaded inverters.

4. The apparatus according to claim 1, further comprising:

- an inverting first output stage coupled to the first pull-up stage to generate a third inverted signal in response to the second inverted signal.

5. The apparatus according to claim 4, wherein the first pull-up stage is capable of providing a variable phase delay to the second inverted signal and the third inverted signal.

6. The apparatus according to claim 5, wherein the second inverted signal and the third inverted signal have approximately the same duty cycle as the input clock signal.

7. The apparatus according to claim 2, wherein the input clock signal, the second inverted signal and the third inverted signal each have approximately a 50% duty cycle.

8. The apparatus according to claim 2, further comprising:

- an inverting second matching stage coupled to the first output stage and responsive to the third inverted signal to generate a fourth inverted signal having a second matching delay, the second matching delay being a difference between a third rise and a third fall propagation time of the second matching stage;

- an inverting second pull-up stage coupled to the second matching stage and responsive to the fourth inverted signal to generate a fifth inverted signal having a second pull-up delay which is substantially reduced by the second matching delay, the second pull-up delay being a difference between a fourth rise and a fourth fall propagation time of the second pull-up stage; and

- an inverting second output stage coupled to the second pull-up stage to generate a delayed clock signal in response to the fifth inverted signal.

9. A system comprising:

- an IC component having a clock generator to generate an input clock signal substantially having a 50% duty cycle; a rise mirror circuit including an inverting first matching stage coupled to the clock generator and response to the input clock signal to generate a first inverted signal with a first changed pulse width; an inverting first pull-up stage coupled to the first matching stage and responsive to the first inverted signal to generate a second inverted signal having a second changed pulse width substantially with a 50% duty cycle, the first pull-up stage being capable of introducing a variable amount of phase shift in the second inverted signal; and

- an automatic test equipment coupled to the first pull-up stage to adjust the variable amount of the phase shift in the second inverted signal.

10. The system according to claim 9, wherein the first changed pulse width substantially equals the second changed pulse width; the first changed pulse width being a selected one of an increased pulse width or a decreased pulse width and the second changed pulse width being the other one of the increased pulse width or the decreased pulse width.

11. The system according to claim 10, wherein the first changed pulse width is the decreased pulse width and the second changed pulse width is the increased pulse width.

12. The system according to claim 9, wherein the first matching stage includes a non-inverting logic element having an input to receive the input clock signal and a NOR gate with one input connected to the input of the non-inverting logic element and another input connected to an output of the non-inverting logic element.

13. The system according to claim 12, wherein the non-inverting logic element includes at least two cascaded inverters.

14. The system according to claim 9, further comprising:

- an inverting first output stage coupled to the first pull-up stage to generate a third inverted signal in response to the second inverted signal.

15. The system according to claim 14, wherein the first pull-up stage is capable of providing a variable phase delay to the inverted second signal and the third inverted signal.

16. The system according to claim 15, wherein the second inverted signal and the third inverted signal have approximately the same duty cycle as the input clock signal.

17. The system according to claim 15, wherein the second inverted signal and the third inverted signal each have approximately a 50% duty cycle.

18. The system according to claim 14, further including:

- a falling mirror circuit including an inverting second matching stage coupled to the first output stage of the rising mirror and responsive to the third inverted signal to generate a fourth inverted signal with a third changed pulse width; an inverting second pull-up stage coupled to the second matching stage and responsive to the fourth inverted signal to generate a fifth inverted signal having a fourth changed pulse width substantially with a 50% duty cycle, the second pull-up stage being capable of introducing a variable amount of phase shift in the fifth inverted signal, and an inverting second output stage coupled to the second pull-up stage and responsive to the fifth inverted signal to generate an output clock signal.

19. The system according to claim 14, the first changed pulse width introduces a duty cycle offset relative to the 50% duty cycle.

20. A method of operating a clock shrink circuit, comprising:

- generating a clock signal with an approximately 50% duty cycle;

- delaying one of the rising and falling edges of the clock signal more than the other edge and inverting the clock signal to generate a first inverted waveform with a first pulse width change;

- using a variable first pull-up stage to delay one of the rising and falling edges of the first inverted waveform more than the other edge and inverting the first inverted waveform to generate a second inverted waveform with a second pulse width change;

- adjusting the first pulse width change to substantially equal the second pulse change to provide the second inverted waveform with an approximately 50% duty cycle; and

- adjusting the first pull-up stage to obtain a selected first phase shift of the second inverted waveform.

21. The method according to claim 20, further comprising:

- inverting the second inverted waveform to generate a third inverted waveform having the first phase shift.

22. The method according to claim 20, wherein delaying one of the rising and falling edges of the clock signal more than the other edge includes introducing a duty cycle offset relative to the 50% duty cycle.

23. The method according to claim 21, further comprising:

- delaying one of the rising and falling edges of the third inverted waveform more than the other edge and inverting the third inverted waveform to generate a fourth inverted waveform with a third pulse width change;

- using a variable second pull-up stage to delay one of the rising and falling edges of the fourth inverted waveform more than the other edge and inverting the fourth inverted waveform to generate a fifth inverted waveform with a fourth pulse width change;

- adjusting the third pulse width change to substantially equal the fourth pulse width change to provide the fifth inverted waveform with an approximately 50% duty cycle; and

- adjusting the second pull-up stage to obtain the selected second phase shift of the fifth inverted waveform.

24. The method according to claim 23, further comprising:

- inverting the fifth inverted waveform to generate an output clock signal having the first and second phase shifts.